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(54) Symmetric bi-directional amplifier.

(57) A transceiver module (10) includes a bi-directional amplifier (16) having a pair of symmetric signal paths for amplification of both transmit and receive signals. The bi-directional amplifier (16) is disposed between a pair of r.f. switches (14, 18) to provide a pair of signal paths between two terminals of the module (10). The amplifier (16) has an input propagation network (30) coupling two input terminals (16a, 16b), and an output propagation network (32) coupling two output terminals (16c, 16d). A plurality of FETs (FET1, FET2, FET3, FET4) have their gates connected to the input propagation network (30) and their drains connected to the output propagation network (32). Electrical paths lengths are selected so that an input signal at one input terminal (16a) propagates with amplification to one output terminals (16c) and an input signal at the other input terminal (16b) propagates with amplification to the other output terminal (16d).

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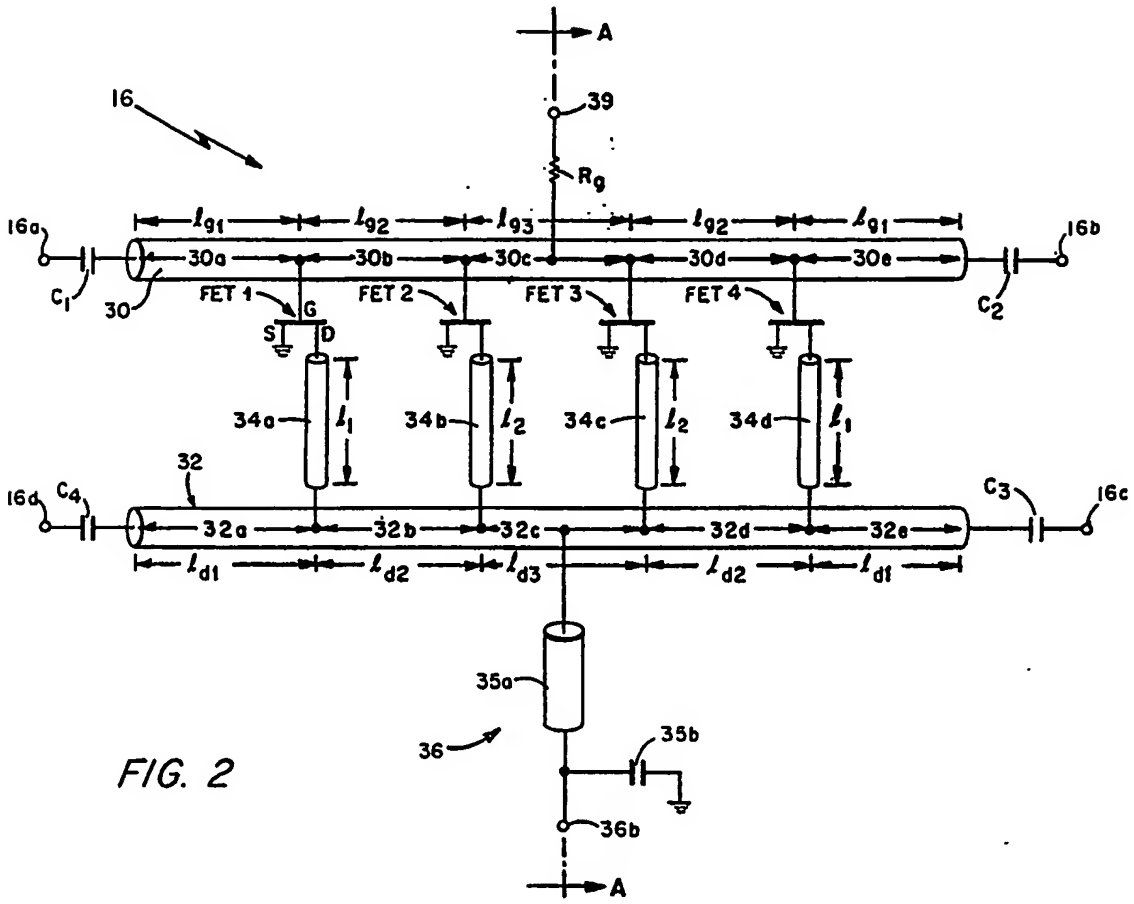
A
16
39
R_g
l_{g1}
l_{g2}
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16a
16b
30a
30b
30c
30d
30e
C_1
C_2
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FET 1
FET 2
FET 3
FET 4
G
S
D
34a
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34c
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l_1
l_2
l_2
l_1
32
16d
C_4
C_3
16c
32a
32b
32c
32d
32e
l_{d1}
l_{d2}
l_{d3}
l_{d2}
l_{d1}
35a
36
35b
36b
A

FIG. 2

SYMMETRIC BI-DIRECTIONAL AMPLIFIER

Background of the Invention

This invention relates generally to radio frequency circuits and more particularly to amplifier circuits.

As is known in the art, distributed amplifiers are used to amplify broadband radio frequency signals. In general, a distributed amplifier includes an input transmission line having a first end coupled to an input terminal of the amplifier, which is used to successively couple input electrodes of a plurality of transistors to such input terminal. The distributed amplifier also includes an output transmission line coupled to an output terminal of the amplifier, which is used to successively couple output electrodes of the transistors to the output terminal. A signal fed to the input terminal propagates along signal paths provided through each one of said plurality of transistors and such output signals from the transistors are added in-phase at the output terminal to provide a composite output signal. The inherent reactance between the input electrode and the reference electrode of each transistor is taken into consideration when designing the input transmission line. A broadband network is provided by incorporating such inherent reactance into the input transmission line. Similarly, inherent reactance between the output electrode of each transistor and the reference electrode is also taken into consideration when designing the output transmission line to provide a broadband output network. Such arrangement enables distributed amplifiers to have very broad operating bandwidths.

It is also known in the art that phased array antennas include a plurality of individual radiating elements. Such elements are typically independently controlled to radiate an electromagnetic signal having a selected phase relationship to the other ones of the electromagnetic signals to provide a composite radiation pattern.

One technique for providing desired phase control of the individual radiating elements uses a transceiver circuit which include separate transmit amplifier and receive amplifiers which are fed respective transmit and receive signal through a common phase shifter. It is also known that it is desired to fabricate such circuits as monolithic microwave integrated circuits. Moreover, it would be preferrable to provide such elements on a single monolithic integrated circuit. It would be desirable therefore to eliminate one of the transmit and receive amplifiers. One technique for achieving this would be to simply provide the amplifier in a common path of the transceiver element and thus steer the radio frequency signals via switches operative during transmit and receive through this common path and thus through the amplifier. One problem with this technique, however, is that it requires four RF switches to provide the common steering path. Thus, again increasing the number of circuit elements in the transceiver. Moreover, the switches also increase the insertion loss and noise figure and decrease the gain, output power and efficiency of the transceiver.

Furthermore, in a transceiver, the receive amplifier is generally optimized for low noise operation, whereas the transmit amplifier is generally optimized for high power operation. Therefore, it would be desirable to provide an amplifier which can be used during both transmit and receive and which also obviates the need for switching circuits. Furthermore, it would be more desirable to provide an amplifier which can be optimized both for low noise operation and high power performance.

Summary of the Invention

In accordance with the present invention, a radio frequency symmetrical, bi-directional amplifier having a pair of input signal terminals and a pair of output signal terminals includes an input propagation network coupled between the pair of input signal terminals of the amplifier. A plurality of transistors, with each transistor having an input electrode and a output electrode, have the input electrodes successively coupled by the input propagation network. The amplifier further includes an output propagation network coupled between the pair of output terminals of the amplifier and being disposed to successively couple the output electrode of each one of the plurality of transistors. The electrical pathlength between a first one of the input terminals and the input electrode of a first one of the transistors is equal to the corresponding electrical pathlength between the second one of the pair of input terminals of the amplifier and the input electrode of a last one of said plurality of transistors. Correspondingly, a second, generally different electrical pathlength between the gate electrode of the first one of the transistors and the gate electrode of the next succeeding one of said transistors is equal to the electrical pathlength between the gate electrode of the last one of said transistors and the gate electrode of a transistor preceding the last one of said plurality of transistors. Similarly, a third, preferrably different electrical pathlength between the first output terminal of the amplifier and the output electrode of the last one of said transistors of the amplifier is equal to the electrical pathlength between a second one of the output terminals of the amplifier and the output electrode of the first one of said transistors. A fourth, different, electrical pathlength between the output electrode of the

preceding one of the transistors and the output electrode of the last one of said transistors is equal to the electrical pathlength between the output electrode of the first one of said transistors and the output electrode of the next succeeding one of said transistors.

Thus, the symmetric bi-directional amplifier provides a pair of signal paths, each having correspondingly equal electrical pathlengths through respective transistors between the input terminal and respective output terminal of the first signal path and the input electrode and output electrode of the second signal path. With such an arrangement, a symmetrical, bi-directional distributed amplifier is provided, which can be incorporated for example into a transceiver module. Such an amplifier can function both as a transmit and receive amplifier while eliminating the necessity for providing switches to steer both transmitted and received signals through a common signal amplifier.

In accordance with a further aspect of the present invention, a radio frequency bi-directional matrix amplifier having a pair of input signal terminals, and a pair of output signal terminals includes an input propagation network coupled between a pair of input signal terminals, and a first plurality of transistors, each transistor having an input electrode and an output electrode with the input electrode of each transistor being successively coupled by the input propagation network. The bi-directional, matrix amplifier further includes an intermediate propagation network disposed to successively couple the output electrode of each one of the first plurality of transistors. A second plurality of transistors are provided with each transistor having an input electrode, a reference electrode, and an output electrode with the input electrode of each of the second plurality of transistors being successively coupled by the intermediate propagation network. An output propagation network is provided to successively couple the output electrodes of each one of the second plurality of transistors, with said output propagation network being successively coupled between the pair of output terminals of the circuit. In a preferred embodiment, the electrical pathlengths between each one of the input terminals of the amplifier and the corresponding one of the output terminals of the amplifier are selected to have correspondingly equal electrical pathlengths. That is, the electrical pathlength between the input terminal and the gate electrode of the first one of the plurality of transistors is equal to the electrical pathlength between the second one of the input terminals of a network and the gate electrode of the last one of the first plurality of transistors. Correspondingly the electrical pathlengths between the gate electrode of a first one of second plurality of transistors and the gate electrode of the next succeeding one of said plurality the transistors is equal to the electrical pathlength between the gate electrode of the last one of said plurality of transistors and the gate electrode of a preceding one of said second plurality of transistors. With this particular arrangement, a matrix, symmetric bi-directional amplifier is provided. A matrixed bi-directional amplifier may have its first stage optimized for low noise and the second and subsequent stages optimized for high power. Such a circuit can satisfy the requirement for low noise for a receive amplifier in a transceiver and high power for a transmit amplifier in the transceiver.

Brief Description of the Drawings

The foregoing features of this invention, as well as the invention itself, may be more fully understood from the following detailed description of the drawings, in which:

FIG. 1 is a schematic representation of a transceiver circuit for use in a phased array antenna in accordance with an aspect of the present invention;

FIG. 2 is a schematic representation of a first embodiment of a bi-directional amplifier for use in the transceiver module of FIG. 1;

FIG. 2A is a schematic representation of an alternate drain bias network for the amplifier of FIG. 2;

FIG. 3 is a schematic representation of an alternate embodiment of a bi-directional amplifier for use in the transceiver module of FIG. 1;

FIGs. 4A and 4B are schematic of matrixed bi-directional amplifiers having alternate bias networks.

FIG. 5 is a block diagram of a recirculating amplifier using the bi-directional amplifier of FIG. 2 or FIG. 3;

FIG. 6 is a block diagram of an amplifying power divider using the bi-directional amplifier of FIG. 2 or FIG. 3;

FIG. 7 is a block diagram of an amplifying power combiner using the bi-directional amplifier of FIG. 2 or FIG. 3; and

FIG. 8 block diagram of an alternate embodiment of a transceiver, particularly for use in high power applications.

Description of the Preferred Embodiments

Referring now to FIG. 1, a transceiver circuit 10 for use in a phased array antenna (not shown) includes

a first r.f. switch 14 and a second r.f. switch 18 to steer an r.f. signal between a pair of terminals 12, 22 of the transceiver 10 through a pair of signal paths 15a, 15b as shown. R.F. switch 14 includes a common port 14a coupled to antenna element 11 via a transmission line 13 and a pair of branch ports 14b, 14c, as shown. Whereas, r.f. switch 18 includes a common port, 18a coupled to a phase shifter 20 via transmission line 19 and a pair of branch ports 18b, 18c, as shown. The common port 14a of switch 14 is coupled to a radiating element 11 at the first terminal 12 of the transceiver circuit 10. Each switch 14, 18 has a control port 14d, 18d, respectively which in response to a control signal fed thereto couples a selected one of the branch ports 14b, 14c of switch 14 and branch ports 18b, 18c of switch 18 to the respective common port 14a, 18a. Preferably, to maintain symmetric impedances through the circuit, such switches 14, 18, and all switches described herein, are terminating switches which present a suitable characteristic impedance at the isolated terminal, to terminate lines fed thereto. The other of said branch ports is substantiall electrically isolated from the common port.

The transceiver 10 is shown to further include a symmetrical bi-directional amplifier 16, as will be described in conjunction with FIG. 2. Suffice it here to say that symmetrical bi-directional amplifier 16 has a pair of input signal terminals 16a, 16b and a pair of output signal terminals 16c, 16d. Amplifier 16 has a first signal path 17a therethrough between input terminal 16a and output terminal 16c and a second substantially electrically identical signal path 17b, between terminal 16b and terminal 16d, as shown. Thus, input terminal 16a of symmetrical bi-directional amplifier 16 is coupled to branch port 14b of r.f. switch 14 whereas, the second output terminal 16d of symmetrical bi-directional amplifier 16 is coupled to branch port 14c of r.f. switch 14. The branch terminals 18b, 18c of r.f. switch 18 are coupled respectively to second input terminal 16b and first output terminal 16c of amplifier 16. The common terminal 18a of r.f. switch 18 is coupled via transmission line 19 to a first input/output port 20a of the phase shifter 20. A second input/output port 20b of phase shifter 20 is coupled to the second terminal 22 of transceiver 10. Phase shifter 20 further has a control port 20c which is responsive to a control signal to impart a selective differential phase shift to a signal propagating through the phase shifter 20. Phase shifter 20 is here a reciprocal phase shifter and may be a reciprocal electronic phase shifter or a ferrite phase shifter or an active phase shifter having reciprocating switches. Examples of phase shifters are described in our U.S. Patent 4,635,062 and our European Patent Application No. 90306267.7.

The output terminal 22 of transceiver 20 is coupled to a utilization system 28 (such as a jammer or radar) which may include a corporate feed network (not shown) for example to distribute signals to the array elements (not shown). Such an arrangement is also described in the above U.S. Patent 4,635,062 and assigned to the assignee of the present invention.

Transceiver 10 operates in a first or transmit mode of operation by coupling a transmit signal between the utilization system 28 and the antenna element 12. Transceiver 10 also operates separately or simultaneously in a second or receive mode of operation, by coupling a signal from the radiating element 12 through the transceiver 10 to the utilization system 28.

In the transmit mode the transmit signal from radar system 28 is fed to the input/output port 20b of here an n-bit phase shifter 20 and in response to a control signal fed along line 28a, to control port 20c provides a selected differential phase shift to the transmit signal propagating therethrough. The differentially phase shifted signal emerges at port 20a and is fed to common port 18a of switch 18. In response to a second control signal fed on control line 28b, a signal path is provided between terminal 18a and terminal 18b of switching means 18 to thus couple the transmit, phase shifted signal to the second input terminal 16b of amplifier 16. The transmit, phase shifted signal is amplified by amplifier 16 and emerges from amplifier 16 at second output terminal 16d. The amplified and phase shifted signal is then fed to the second branch terminal 14c of the first switch 14 and in response to a third different control signal fed via line 28c to port 14d of switch 14, a signal path is created between port 14c and port 14a of switch 14 thus coupling said signal to radiating element 11.

Correspondingly, in a receive mode, a receive signal is fed from radiating element 11 and coupled to the common port 14a of steering means 14. In response to a complimentary state of the control signal fed on line 28c, a second, different signal path is provided between a common port 14a and first branch port 14b, thus feeding the received signal to the first input terminal 16a of amplifier 16. An amplified, receive signal appears at the first output terminal 16c of amplifier 16 and is fed to the second branch port 18c of switch 18. In response to a complimentary state of control signal fed on line 28b, a signal path is provided between terminal 18c and common terminal 18a. The signal is thus fed from terminal 18a to terminal 20a of the phase shifter 20. A second, relative differential phase shift is provided to the amplified received signal. The second relative phase shift is generally the same phase shift applied to the signal during the transmit mode. If desired, the relative phase can be altered by feeding a different control signal to port 20c along control line 28a. At the second input/output 20b of phase shifter 20, said signal is thus coupled to the

second terminal of the transceiver circuit 22 and to the radar system 28 to be utilized and analyzed by the utilization system 28 in some known or predetermined manner.

Referring now to FIG. 2, a schematic representation of a symmetrical bi-directional amplifier 16 for use in the transceiver element 10 as described in conjunction with FIG. 1 is shown to include an input propagation network 30 having a first plurality of transmission line sections 30a-30e used to successively couple gate electrodes G of a plurality of field effect transistors FET 1 to FET 4 as shown. The symmetrical bi-directional amplifier 16 further includes an output propagation network 32 here comprised of a second, corresponding plurality of transmission line sections 32a-32e used to successively couple drain electrodes D of the field effect transistors FET 1 to FET 4. Preferably, third transmission line sections 34a-34d are disposed between drain electrodes FET 1 - FET 4 and the common output propagation network 32, as also shown. The input propagation network 30 is coupled via d.c. blocking $_1$capacitors C_1, C_2 to a pair of input terminals 16a and 16b of the amplifier. A d.c. gate bias voltage is here fed at the center point of transmission line 30 via a high impedance resistor Rg or a high inductance value series inductor (not shown). Gate bias voltage is provided to a gate bias terminal 39 through resistor Rg to properly bias the gates of the field effect transistors as is commonly known. Similarly, the output propagation network 32 is coupled via d.c. blocking capacitors C_3, C_4 to a pair of output terminals 16c and 16d of the circuit 16, as shown. Drain bias is here provided, via a network 36 which includes a quarter wavelength transmission line stub 35a which has an electrical pathlength corresponding to a quarter wavelength at the nominal or center frequency of the operating bandwidth of the amplifier, and a r.f. bypass capacitor 35b coupled between said stub 35 and ground, as shown. A drain bias d.c. voltage is fed to terminal 36b to properly bias the drains of each of the field effect transistors FET 1 - FET 4, as shown.

An alternative to the bias arrangement described for the drain electrode is shown in FIG. 2A and includes a conventional ladder network having a resistor disposed in a capactively coupled shunt path to ground. Here, such a ladder network would be preferred for broadband matching and thus operation of the distributed, symmetrical bi-directional amplifier and would be coupled prior to the connection of d.c. blocking capacitor C_3, for example, with the output propagation network 32. That is, terminal 36b' of the ladder network is coupled at the connection of the capacitor C_3 with the propagation network 32, as would be generally known. Preferably, in order to maintain symmetrical operation of the amplifier as will be described, two of such networks 36' (FIG. 2A) would be provided, one at either end of the output propagation network 32. Only one of such networks need be fed a D.C. bias voltage.

The bi-directional, distributed amplifier 16 shown in FIG. 2 is different than conventional distributed amplifiers, here each end of the propagation network serves as either an input terminal or an output terminal for the circuit. Such networks are not terminated in a characteristic impedance. A pair of substantially identical paths is provided between terminals 16a and 16c and terminals 16b and 16d. That is, in operation the amplifier provides substantially the same gain and phase characteristic to signals propagating between terminal 16a-16c as it does between terminals 16b and 16d. Such operation is provided by designing the amplifier to be symmetrical with respect to impedance, and electrical pathlength characteristics about a central portion of the amplifier, as denoted by the line AA. That is, proceeding from line AA, the length of the transmission line 30c is bifurcated such that a first half of said line has electrical pathlength of $\ell_{g3}/2$ and a second half of said line has identical pathlength of $\ell_{g3}/2$. The next pair of sections transmission lines 30b, 30d each have identical pathlength of ℓ_{g2} and the succeeding pair of sections of transmission line $\ell 30_a$ and $\ell 30_e$ have identical electrical pathlength of ℓ_{g1}. Similarly, at the output propagation network, the network is symmetrical about line AA and proceeding from line AA, the transmission line section 32c has a pair of identical half electrical pathlengths $\ell_{d3}/2$, as shown. Sections 32b and 32d have identical electrical pathlengths of ℓ_{d2}, whereas sections 32a and 32e also have identical electrical pathlengths of here ℓ_{d1}. Drain electrodes D of each transistor FET 1 - FET 4 are coupled to line 32 via transmission lines 34a-34d having lengths ℓ_1, ℓ_2, ℓ_2, and ℓ_1, respectively.

In practice lengths ℓ_{g1}, ℓ_{g2}, and ℓ_{g3} and ℓ_{d1}, ℓ_{d2}, and ℓ_{d3} may be different, and are selected to optimize signal propagation to one of said pair of output terminals and minimize gain ripple. Thus, a signal fed from terminal 16a through the field effect transistors FET 1 - FET 4 will propagate along a path having an identical electrical pathlength as a signal fed from terminal 16b to terminal 16d. Moreover, the lengths ℓ_{g1} - ℓ_{g3}, ℓ_1, ℓ_2, and ℓ_{d1} - ℓ_{d3} of transmission lines 30a-30e and 32a-32e are selected to provide equal electrical pathlengths between terminal 16a and terminal 16c through each of said field effect transistors FET 1 - FET 4, as would commonly be done in a conventional distributed amplifier. Here, however, since the distributed amplifier 16 is also symmetrical about the line AA by use of the transmission line length as shown, equal electrical pathlengths are also provided between terminal 16b and 16d through each one of the paths provided by the field effect transistors FET 1 - FET 4. This arrangement permits a signal to be fed to terminal 16a, propagate along lines 30a-30e, and have successive portions fed to gate electrodes G of

transistors FET 1 - FET 4. In response successive signal portions are coupled from drain electrode D thereof and propagate along line 32 and add up in phase at terminal 16c and provide a partial null signal at terminal 16d. Similarly, a signal coupled to terminal 16b has successive portions thereof fed through transistors FET 4 - FET 1 to provide amplified portions at the drain electrode of said transistors, which add in phase at terminal 16d and provide a partial null signal at terminal 16c. Thus, a symmetrical bi-directional distributed amplifier is provided. Moreover, since the electrical pathlength between terminal 16a and 16c through field effect transistor FET 1 is identical to the electrical pathlength between terminal 16b and 16d through field effect transistor FET 4, as is the other corresponding sets of electrical pathlengths between said terminals, the amplifier will have substantially identical characteristics whether the signal is fed between terminal 16a and 16c or whether said signal is fed between terminal 16b and 16d.

A design example for the amplifier 16 as shown in FIG. 2 is described in conjunction with the accompanying table and description below:

Table of Electrical Pathlengths

$\ell_{g1} = 0.396_{mm}$	$\ell_{d1} = 0.902_{mm}$	$\ell_1 = 0.117_{mm}$
$\ell_{g2} = 0.858_{mm}$	$\ell_{d2} = 1.468_{mm}$	$\ell_2 = 0.240_{mm}$
$\ell_{g3} = 0.986_{mm}$	$\ell_{d3} = 1.296_{mm}$	

The circuit is designed to be fabricated on a substrate of gallium arsenide having a thickness of 0.1 mm. The transmission line sections may be fabricated as lengths of microstrip transmission line or to conserve space are alternatively fabricated as spiral inductors. Moreover, lumped element lines or artificial lines may alternatively be used. The line lengths shown in the table are for field effect transistors FET 1 - FET 4 each having 200 mm of total gate periphery. The input transmission line inductor width is 0.01 mm whereas the output transmission line conductor width is 0.02 mm.

Referring now to FIG. 3, an alternate embodiment 16' of a symmetrical bi-directional amplifier, here a matrixed, symmetrical bi-directional amplifier is shown to include a pair of input terminals 16a', 16b', a pair of output terminals 16d' , 16c' , a first plurality of field effect transistors FET 11 - FET 14, and a second plurality of field effect transistors FET 21 - FET 24. Here, the pair of input terminals 16a', 16b' are coupled by an input propagation network 50 comprised of here inductors preferably spiral inductors 50a-50e. Here, spiral inductors 50a-50e provide electrical pathlengths of ℓ_{11}, ℓ_{12}, ℓ_{13}, ℓ_{12}, and ℓ_{11}, respectively, as shown. Said propagation network 50 is shown to successively couple the gate electrodes G of the field effect transistors FET 11 - FET 14 to provide the respective electrical pathlengths between said gate electrodes as shown.

The output or drain electrodes of the field effect transistors FET 11 - FET 14 are coupled via inductors 54a-54d, respectively, to a second or intermediate propagation network 52 comprised of inductors preferrably spiral inductors 52a-52e, as also shown. The spiral inductors 52a-52e provide electrical pathlengths of ℓ_{21}, ℓ_{22}, ℓ_{23}, ℓ_{22}, ℓ_{21}, respectively. Here said transmission line network 52 provides an output coupling network to successively couple the output electrodes of the transistors FET 11 - FET 14, as well as, provide an input coupling network to successively couple the input or gate electrodes of the second plurality of field effect transistors FET 21 - FET 24. The output electrodes of the second plurality of field effect transistors are coupled via inductors 58a - 58d having electrical lengths of ℓ_{d21}, ℓ_{d22}, ℓ_{d22}, ℓ_{d21}, respectively, and an output transmission network 56 comprised of sections 56a-56e, as shown. Here each of said transmission line sections have electrical pathlengths of ℓ_{31}, ℓ_{32}, ℓ_{33}, ℓ_{32}, ℓ_{31}, respectively. Thus, the electrical pathlength of each one of the transmission line sections is selected to provide a network which is symmetrical about the line AA as also shown and described above in conjunction with FIG. 2.

Here, however, a low noise high power symmetrical bi-directional amplifier having low gain ripple is provided, which is particularly desirable when the amplifer 16' is used in transceiver applications. The matrix amplifier 16' is equivalent to a pair of cascaded bi-directional amplifiers. In transceiver applications, such as described in conjunction wit FIG. 1, it is most desirable to have a low noise amplifier as the first amplifier in the receive channel or path. With the bi-directional matrix amplifier 16', the first stage or first plurality of transistors FET 11 - FET 14 are fabricated and selectively designed to provide a relatively low power, low noise amplifier stage. During a receive mode of operation, the first stage of amplification in the receive channel or path is a low noise amplification stage. The second stage of the matrix bi-directional

amplifier 16' shown in FIG. 3 is designed to provide high power. This is also desirable in receive mode since it reduces further amplification requirements in the radar system. During transmit mode this is also desirable for use in the transceiver module 10 (FIG. 1) to provide a higher power transmit signal to the radiating element 11.

Additional stages of matrixed/distributed amplification may be provided to the circuit shown in FIG. 3 to provide higher output power and gain. Accordingly, a three stage matrix distributed amplifier may be provided using the similar arrangement as described for that in FIG. 3.

Here, electrical signal paths between the input terminal 16a', for example, and output terminal 16c' include the same path as that described in conjunction with FIG. 2, as well as, additional paths created by the matrix or cascade matrix of the pair of amplifying stages. For example, an input signal fed to input terminal 16a' has successive portions which are coupled to each one of the gate electrodes of the field effect transistors FET 11 - FET 14. The transistors FET 11 - FET 14 are responsive to said signal portions and provide in response a corresponding plurality of output signal at the drain electrodes D thereof. The output signal portions propagate along the intermediate propagation network 52. A pair of portions of each of said output signal portions propagates along the propagation network 52 towards each end. In the direction towards the end portions 52" of the network 52, such signals add in phase to provide a travelling wave as is commonly known in distributed amplifiers. At the opposite end, 52' of the propagation network 52, the waves somewhat distructively interfere. Here, however, in addition to the output signals propagating along the propagation network 52 and adding in succession to provide a signal at the end 52", said portions of said signals are also successively coupled to the second plurality of field effect transistors FET 21 - FET 24 to provide corresponding output signals at the drain electrodes thereof which likewise, successively propagate along the output network 56. Thus, an input signal fed to terminal 16a' provides an output signal at terminal 16c' which is amplified by both the additive gain associated with the coupling of successive portions of said signals through the stages of distributed amplifier, as well as, the multiplicative gain associated with coupling said signal through respective cascaded transistors.

Bias networks are provided to the amplifier 16' as shown. Gate bias is provided to FET 11 - FET 14, via the input propagation network 50 by a high value resistor R coupled at here preferably the center of the network 50. Gate bias V is fed to such resistor R at terminal 58a. Drain bias for FET 11 - FET 14 is here provided at the terminals 52' and 52' ' of propagation network 52 by bias networks 36 as described in conjunction with FIG. 2 or the broadband ladder network 36' as described in conjunction with FIG. 2A. These networks provide drain bias to the drain electrodes D of the field effect transistors FET 11 - FET 14. A separate gate bias needs to also be provided to the second set of field effect transistors FET 21 - FET 24. Here said gate bias (V_g) is provided by D.C. blocking capacitors C disposed to couple the gate electrodes to the propagation network 52 and separate pull up resistors R as also shown. Here the value of said capacitors C is relatively large to provide an essentially AC short circuit path between the gate electrode and the transmission network 52. A third drain bias network 57 is also provided to bias the output network 56. Here said third drain bias network 57 includes a quarter wavelength stub 57a and shunt mounted capacitor 57b, as described for network 36 (FIG. 2) coupled at the center of the propagation network 56. Alternatively, bias circuits may be provided at each end of the network 50, as well as, each end of the network 56 to maintain a symmetric impedance characteristic about line AA of the distributed amplifier.

Referring now to FIGS. 4A and 4B, alternative biasing networks for the matrix bi-directional distributed amplifier 16' of FIG. 3 are shown.

Referring now to FIG. 4A, a matrixed distributed, bi-directional amplifier 16' ' having an alternate biasing arrangement is shown to include here two sets of field effect transistors FET 11 - FET 15 and FET 21 - FET 25, have each set having five transistors connected in a matrix cascade as generally described in conjunction with FIG. 3, except for the presence of an extra transistor in each set of said transistors. The amplifier 16' ' includes an input network 50' here substantially similar to input network 50 of FIG. 3 except that said network has an extra element 50f to inter-connect FET 15 and thus the sections have electrical pathlengths of ℓ_{g11}, ℓ_{g12}, ℓ_{g13}, ℓ_{g13}, ℓ_{g12}, and ℓ_{g11}, respectively as shown. An intermediate propagation network 52 is also included in said amplifier 16" and is used to successively and matrixly couple the output or drain electrodes D of the transistors FET 11 - FET 15 to the input or gate electrodes G of a second set of transistors FET 21 - FET 25. Here, network 52 is substantially similar to network 52 of FIG. 3 except for the addition of an extra element 52f and such sections have electrical pathlengths of ℓ_{21}, ℓ_{22}, ℓ_{23}, ℓ_{23}, ℓ_{22}, and ℓ_{21}, respectively. The drain electrodes of transistors FET 11 - FET 14 are coupled to the intermediate propagation network 52 via lines 54a-54e, having lengths of ℓ_{d11}, ℓ_{d12}, ℓ_{d13}, ℓ_{d12}, ℓ_{d11}, respectively. Output propagation network 56' is used to successively couple the output or drain electrodes of the field effect transistors FET 21 - FET 25 between a pair of output terminals 16d' , 16c' , as also shown. Such network is

similar to network 56 (FIG. 3), except for the additional section 56f and thus such sections have lengths of ℓ_{31}, ℓ_{32}, ℓ_{33}, ℓ_{33}, ℓ_{32}, ℓ_{31}, respectively. The drain electrodes of transistors FET 21 - FET 25 are coupled to the output propagation network 56 via transmission line sections 58a-58e having lengths ℓ_{d21}, ℓ_{d22}, ℓ_{d23}, ℓ_{d22}, ℓ_{d21}, respectively. Here the gate electrodes of the second set of transistors FET 21 - FET 25 are coupled to the intermediate propagation network 52 via transmission line sections 59a-59e, as shown. These optional transmission line sections 59a-59e may be desirable in certain layouts of the matrix distributed amplifier particularly when fabricated as a monolithic microwave integrated circuit. These sections have lengths of ℓ_{g21}, ℓ_{g22}, ℓ_{g23}, ℓ_{g22}, ℓg21, respectively.

The amplifier 16' ' is provided gate bias to transistors FET 11 - FET 15 via a network 62 which is coupled to the center of the input propagation network 50' and includes a shunt bypass capacitor and a voltage divider network comprised of a pair of resistors (not numbered). Similarly, the drain bias is provided to the output network 56' and thus to the drain electrodes of the second set of transistors FET 21 - FET 25 by a network 63 which here includes an inductor disposed in shunt across resistor R coupled to a shunt mounted r.f. bypass capacitor C which is coupled thereby to the center of the propagation network 56'. Alternatively, the network 36 (FIG. 2) may be used. Gate bias is provided to the second set of field effect transistors FET 21 - FET 25 as is drain bias provided to the first set of transistors FET 11 - FET 15 via a network 70 comprised of inductors L_{B1} - L_{B6}, and D.C. blocking capacitors C_{d1} - C_{d5} disposed between the source electrodes of transistors FET 21 - FET 25 and ground as shown. The gate bias/drain bias network further includes a pair of capacitively isolated resistor shunt paths comprised of resistors R_1, R_2 and capacitors C_5, C_6 mounted in respective series networks (not numbered) between the ends 52' 52" of intermediate transmission line 52 and ground. A D.C. current path is provided through transistors FET 21 - FET 25 via inductors ℓ_{B1} - ℓ_{B6}, whereas to a.c. or microwave frequency signals, these inductors provide a high impedance and thus isolation between the transistors FET 21 - FET 25 and FET 11 - FET 15. The capacitors C_{d1} - C_{d5} provide, at radio frequency signals, an r.f. ground for each of the transistors FET 21 - FET 25, thus permitting the gates of the second set of transistors and the drains of each of the first set of transistors to be D.C. biased. One drawback with this bias arrangement, however, is that the transistors FET 21 - FET 25 are required to run at a bias determined by I_{DSS}. Thus, amplifier performance will be sensitive to the gate voltage applied to the first set of transistors, since both sets of transistors must operate at the same drain current. Thus minor variations in processing between transistors may cause problems in biasing.

Referring now to FIG. 4B, an alternative embodiment of a biasing network to overcome the bias sensitivity described above is shown. Here amplifier 16'" includes substantially the same components as described above for amplifier 16", and thus such like components are not numbered in FIG. 4B except for those specifically mentioned herein. The bias network for the amplifier 16'" includes a pair of resistor divider networks 72, 74 here each being comprised of four resistors R1-R4. Also, coupled to the end of the output propagation network 56" are here a pair of drain bias networks 63a and 63b of the type generally described in conjunction with FIG. 4A for network 63. Here said networks are coupled between the ends of propagation network 56" and the connection with the external D.C. blocking capacitor C_3, C_4. Each of the voltage divider networks 72, 74 is coupled between its respective drain bias network 63a, 63b or 36 (FIG. 2) and the input propagation network 50" as shown. Although only one of said voltage divider networks 72, 74 is needed to provide bias to the respective transistors, a pair of such voltage divider networks. 72, 74 are preferred here to insure that impedance of the amplifier will be symmetric about the line AA. Each of the voltage dividers is disposed across both of the sets of field effect transistors FET 11 - FET 15 and FET 21 - FET 25, as shown, to insure that both sets of field effect transistors operate at the same gate to source voltage. The amplifier, therefore, can operate over a much wider range of gate bias voltages.

Referring now to FIGS. 5-7, alternative applications for the bi-directional amplifier 16-16'" (FIGS. 2, 3, 4A, 4B) are shown. Referring first to FIG. 5, a recirculating amplifier 80 is shown to include here a pair of circulators 82, 84 each of which has three ports 82a-82c, 84a-84c, respectively with ports 82c and 84c herein being terminated in characteristic impedance Z . The circulators 82 and 84 are coupled to one of the bi-directional amplifier 16-16'" as described in conjunction with FIGS. 2, 3, 4A, and 4B. Thus, any one of the embodiments of the bi-directional amplifier may be used. Using amplifier 16 as an example, one of the input terminals 16a of the bi-directional amplifier 16 is coupled to one of the ports here 82b of circulator 82. The corresponding output terminal of said amplifier 16 that is the first output terminal 16c is coupled to one of the ports 84a of circulator 84. A second one of said ports of circulator 84 here port 84b is coupled to the second input terminal 16b. The second output terminal 16d of the amplifier 16 provides the output terminal 81b of the recirculating amplifier 80. Thus, a signal fed at input terminal 81a of the amplifier 80 is coupled between port 82a and 82b of circulator 82, fed to the input of the first amplifier path of bi-directional amplifier 16, coupled through the second circulator 84 via ports 84a and 84b and is recirculated back to amplifier 16 through the second amplifier path of amplifier 16 between terminal 16b and 16d. Thus, two

stages of amplification are provided to the input signal fed at terminal 81a while using only one amplifier circuit.

Referring now to FIG. 6, an amplifying power divider 90 is shown to include a power divider circuit 92 here such as, for example, a Wilkinson power divider or other similar circuits having an input port 92a which provides at a pair of output ports 92b, 92c thereof, a pair of equal amplitude in phase signals. Said signals are fed to the input terminals 16a, 16b of one of the aforementioned bi-directional amplifiers 16-16''' (FIGS. 2, 3, 4A, and 4B). At the output terminals of said amplifier 16, for example, are accordingly provided pair of equal amplitude, in phase output signals which have been amplified and thus provided gain and power in accordance with the characteristics of the amplifier 16.

Referring now to FIG. 7, an amplifying power combiner 95 is shown to include one of the amplifiers 16-16''' (FIGS. 2, 3, 4A, and 4B) here amplifier 16 having a pair of input terminal 16a, 16b which are fed a pair of input signals and a pair of output terminals 16c, 16d which are coupled to a pair of common ports 96b, 96c of a power combiner/divider of the Wilkinson type or other varieties as described in conjunction with FIG. 6. The common terminal 96a of the power combiner 96 provides the output terminal for the amplifying power combiner. Thus, a pair of input signals are fed at terminals 16a, 16b of amplifier 16, propagate through the pair of amplifying chains in said amplifier and appear at the output terminals 16c, 16d of said amplifier. The output signals are then coupled and combined together to provide a composite output signal at terminal 96a.

Referring now to FIG. 8, an alternative embodiment of a transceiver 60 is shown as having a first input/output terminal 62 and a second input/output terminal 86, as shown, The first terminal 62 is coupled to a radiating element 11. The transceiver further includes a first RF switch 64, here a terminating RF switch, as described in conjunction with FIG. 1, having a common port 64a and a pair of branch port 64b, 64c, as also described in conjunction with FIG. 1 for switch 14. The transceiver further includes a pair of quadrature couplers 66, 67 used to couple a pair of amplifiers stages 65a, 65b to provide a balanced amplifier path. Couplers 66 includes a pair of input terminals 66a, 66b, with terminal 66a coupled to terminal 64c of switch 64, and terminal 66b coupled to a first single-pole/single-throw switch 72. Outputs 66c, 66d of coupler 66 are coupled to respective amplifier stages 65a, 65b, here said amplifiers being any conventional amplifier and preferrably being linear high power amplifier stages. The outputs of said amplifier stages 65a, 65b are coupled to the ports 67a, 67b of coupler 67. A first output port 67c of coupler 67 is coupled to the branch port 64b of switch 64 and a second one of the output port 67d of coupler 67 as coupled to a second single-pole/single-throw switch 73, here also a terminating switch. Switches 72, 73 provides a first set of recipricating switches to steer signals through cascaded paths. The second terminals of switches 72 and 73 are coupled respectively to the input and output ports of a second pair of quadrature couplers 70 and 69 as shown. Here the interconnections of said couplers 70 and 69 and amplifier stages 68a and 68b are substantially similar as described above for couplers 66, 67 and amplifier stages 65a, 65b.

Here said couplers 69 and 70 provide a pair of output terminals and input terminals respectively for the coupled amplifier chain. Thus, the first output terminal 69c of coupler 69 is coupled to the second end of switch 72, the second output terminal 69d of coupler 69 is coupled to one end of a third single-pole/single-throw switch 74, whereas the input terminal 70a of coupler 70 is connected to switch 73. The second input terminal 70b of coupler 70 is connected to switch 75, as also shown. Switch 74 and switch 75 are a second set of recipricating switches and are coupled respectively to an input propagation network 78a and an output propagation network 78b of a bi-directional distributed amplifier 78, having successively coupled field effect transistors 78c, and as described in conjunction with FIG. 2. A third pair of single-pole/single-throw switches 79, 80 are used to cascade interconnect the amplifier stage 78 with a second amplifier stage 81, here also having an input propagation network 81a and output propagation network 81b successively interconnecting a plurality of transistors 81c, and being of the type as generally described in conjunction with FIG. 2.

The other ends of said propagation networks 81a, 81b are coupled to branch ports of the second single-pole/double-throw terminating switch 82. Common port 82a thereof is coupled to a phase shifter 84, as also described in conjunction with FIG. 1. The other port of the phase shifter 84 is coupled to the second terminal 86 of the transceiver 60.

In operation, a signal is fed between terminal 86 to the radiating element 11 in a transmit mode, for example, or from radiating element 11 to terminal 86 in a receive mode. Using the transmit mode as representative of the operation of the circuit with solid arrows denoting the signal path during transmit, a signal is fed through the phase shifter 84 and is provided with a selected differential phase shift. The phase shifted signal is then fed from the phase shifter 84 to the common port 82a of switch 82. In response to a control signal fed to a control port 82d the common port 82a is coupled to the branch port 82c. The signal is thus fed to the input propagation network 81a of amplifier 81. The signal is successively fed through the

transistors 81c to the output propagation network 81b and is fed to the output terminal thereof, which is here coupled to single-pole/single-throw switch 79. Thus, in this mode of of operation, single-pole switch 79 is in a closed position where single-pole/single-throw switch 80 is in an open position, as shown. The signal is fed through switch 79 to input propagation network 78a of amplifier 78 and is again successively coupled through the plurality of transistor elements 78c to the output propagation network 78b. Such signal is fed from output propagation network 78b to the single-pole/single-throw switch 75, which is in a closed position with single-pole/single-throw switch 74 being in an open position. The signal is then fed to terminal 70b of coupler 70. At terminals 70c, 70d of coupler 70, a pair signal portions, equal in magnitude and in quadrature are provided, and coupled to the amplifiers 68a, 68b. The signal component at amplifier 68a here is being shifted by a 90° phase shift relative to the phase of signal component at amplifier 68b. Said signal components propagate through the amplifiers 68a, 68b are amplified and emerge at the outputs of the amplifiers 68a , 68b. The amplified signal portions are fed to the second coupler 69. Here coupler 69 is arranged with respective coupler 70, such that said amplified, quadrature signals add in-phase at terminal 69c and cancel at terminal 69d. Thus at terminals 69c, the amplified high-powered signal is coupled to the single-pole/singlethrow switch 72, which is closed, and is fed to couplers 66, 67, and amplifiers 65a, 65b. The signal propagates through quadrature couplers 66, 67 and amplifier stages 65a, 65b, in a similar manner is for couplers 69, 70, here emerging at terminal 67c of coupler 67 and is fed to the branch port 64b of switch 64. Similarly, in response to a control signal fed to a port 64d, switch 64 couples its common port 64a to the branch port 64b thus providing a path between the coupler 67c and the radiating element 11. Each of the single-pole/single throw switches pairs 72, 73; 74, 75; and 79, 80 are controlled by control signals (not shown) as would be apparent to one of skill in the art.

The pair of quadrature couplers and the pair of amplifier chains for each of the high power stages 65a, 65b are inter-connected to steer a signal through a balanced symmetric, high power amplifier stage.

Thus, using couplers 66, 67 and amplifiers 65a, 65b as an example, for a receive mode, a signal is fed to terminal 66a of coupler 66, with terminal 66c being the in-phase terminal and terminal 66d being the quadrature terminal. Thus at terminal 66d, a signal having -90° relative phase shift is provided, whereas at terminal 66c, such signal has a relative phase shift of 0°. These signals propagate through the pair of identical amplifiers, 65a, 65b and emerge therefrom with the -90° relative phase difference. The signal from amplifier 65a is fed to terminal 67a, said terminal being the in-phase terminal, whereas the signal from amplifier 65b is fed to the quadrature terminal 67b. At the outputs of coupler 67 therefor, a pair of composite signals are provided. A first one of component signals from amplifier 65a has a first component, which is fed to terminal 67a with a relative phase shift of -90° at terminal 67d and 0° at terminal 67c. The components from amplifier 65b are likewise fed to terminal 67b, and provide a relative phase shift of -90° at terminal 67d and a relative phase of -180° at terminal 67c. Thus, at terminal 67c such signals add substantially out of phase and thus cancel each other, whereas at terminal 67d, such signals add in-phase and to propagate through switch 73 in the receive mode of operation. A similar arrangement is provided with coupler 69 and 70 and amplifier stages 68a, 68b. Moreover, during transmit mode, such an arrangement also holds. The embodiment shown in FIG. 8 is particularly desirable for applications where noise characteristics are relatively unimportant in comparison to providing high power, such as in electronic countermeasures applications. For applications where noise considerations are important, the circuit as shown in FIG. 1, using the bi-directional amplifiers of FIG. 2 or 3 is generally preferrable.

Having described preferred embodiments of the invention, it will now become apparent to one of skill in the art that other embodiments incorporating their concepts may be used. It is felt, therefore, that these embodiments should not be limited to disclosed embodiments, but rather should be limited only by the spirit and scope of the appended claims.

Claims

1. A radio frequency bi-directional amplifier having a pair of input signal terminals and a pair of output signal terminals comprising:
   an input propagation network coupled between the pair of input signal terminals of the amplifier;
   a plurality of transistors, each transistor having an input electrode and an output electrode, with the input electrode of each transistor being successively coupled by said input propagation network; and
   an output propagation network coupled between the pair of output terminals of the circuit and being disposed to successively couple the output electrode of each of the plurality of transistors with said propagation networks each having predetermined electrical pathlengths between respective successively coupled input electrodes and output electrodes, and with the electrical pathlengths between a

first one of the input terminals and the input electrodes of a first one of the transistors being equal to the corresponding electrical pathlength between the second one of the pair of input terminals of the amplifier and the input electrode of a last one of said plurality of transistors, and with the electrical pathlength between the first one of the output terminals of the amplifier and the output electrode of the last one of said transistor being equal to the electrical pathlength between a second one of the output terminals of the amplifier and the ouput electrode of the first one of said transistors.

2. The bi-directional amplifiers are cited in Claim 1, wherein each one of said transistors includes inherent reactance between the input electrode and a grounded electrode of said transistor, which in combination with the input propagation network provides a network having a predetermined characteristic impedance.

3. The bi-directional amplifiers are cited in Claim 1, wherein each one of said transistors includes inherent reactance between the output electrode and a grounded electrode of said transistor, which in combination with the output propagation network provides a network having a predetermined characteristic impedance.

4. The radio frequency amplifier are cited in Claim 1, wherein said transistors are field effect transistors.

5. A radio frequency bi-directional amplifier having a pair of input signal terminals and a pair of output signal terminals comprising:
an input propagation network coupled between the pair of input terminals of the amplifier;
a first plurality of transistors, each transistor having an input electrode and an output electrode, with the input electrode of each transistor being successively coupled by said input propagation network;
an intermediate propagation network disposed to successively couple the output electrode of each one of the first plurality of transistors;
a second plurality of transistors, each transistors having an input electrode, a reference electrode, and an output electrode with the input electrode of each of the second plurality of transistors being successively coupled by the intermediate propagation network; and
an output propagation network coupled between the pair of output terminals of the circuit being disposed to successively couple the output electrode to each of the second plurality of transistors.

6. The amplifier as recited in Claim 5, wherein the electrical pathlength between the first one of the output terminals of the amplifier and the output electrode of the last one of said transistors being equal to the electrical pathlength between a second one of the output terminals of the amplifier and the ouput electrode of the first one of said transistors.

7. The bi-directional amplifiers are cited in claim 6, wherein each one of said transistors includes inherent reactance between the input electrode and a grounded electrode of said transistor, which in combination with the input propagation network provides a network having a predetermined characteristic impedance.

8. The bi-directional amplifiers are cited in Claim 6, wherein each one of said transistors includes inherent reactance between the output electrode and a grounded electrode of said transistor, which in combination with the output propagation network provides a network having a predetermined characteristic impedance.

9. The radio frequency amplifier are cited in Claim 6, wherein said transistors are field effect transistors.

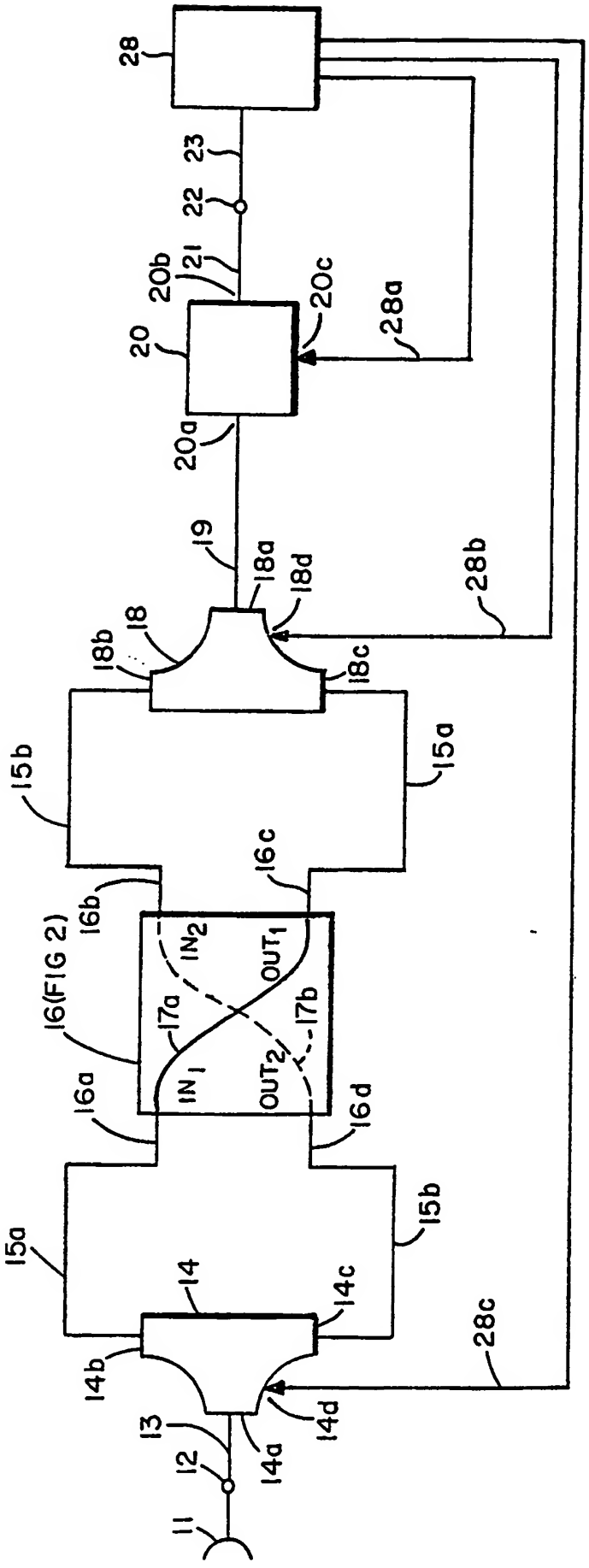
28
23
22
21
20b
20c
28a
20
20a
19
18a
18d
28b
18
18b
18c
15b
15a
16c
16b
16(FIG 2)
IN2
OUT1
17a
17b
IN1
OUT2
16a
16d
15b
15a
14
14c
28c
14b
14d
13
12
14a
11
10

FIG. 1

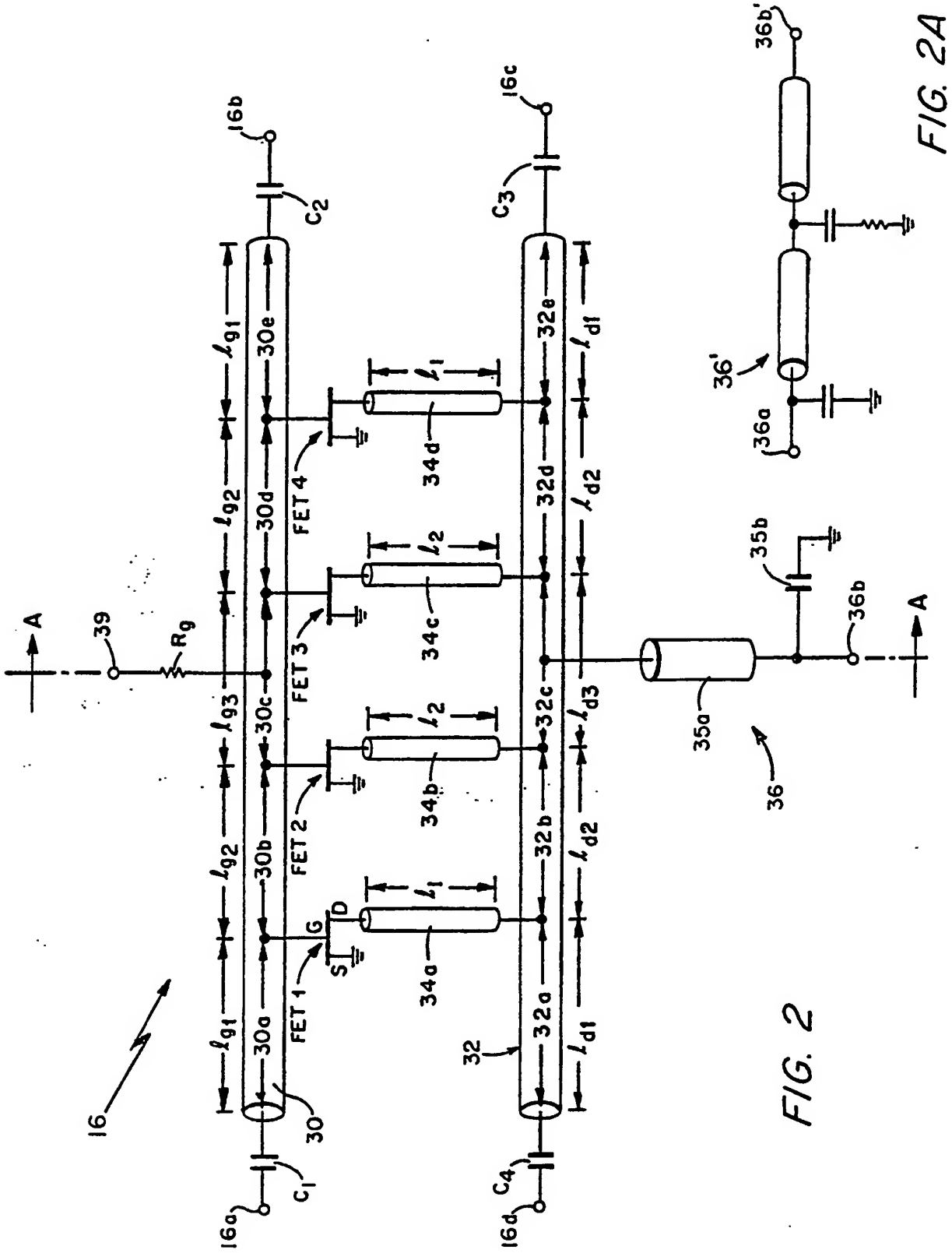
16
16a
16b
16c
16d
C1
C2
C3
C4
30
30a
30b
30c
30d
30e
32
32a
32b
32c
32d
32e
34a
34b
34c
34d
FET 1
FET 2
FET 3
FET 4
G
D
S
39
Rg
A
35a
35b
36
36'
36a
36b
36b'

FIG. 2

FIG. 2A

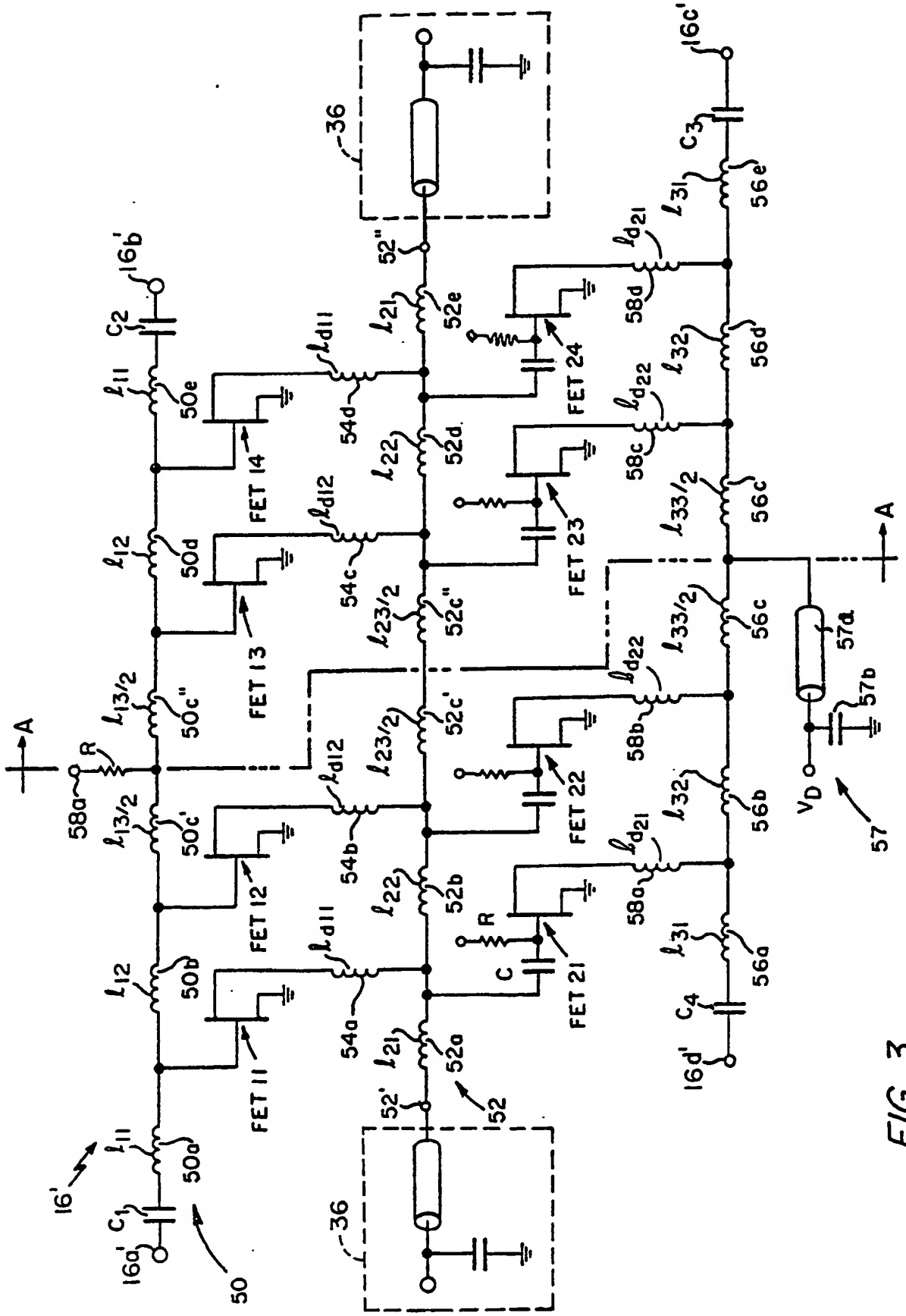
16'
16a'
C1
l11
50a
50
l12
50b
l13/2
50c'
l13/2
50c"
l12
50d
l11
50e
16b'
C2
16c'
C3
l31
56e
l32
56d
l33/2
56c
l33/2
56c
l32
56b
l31
56a
C4
16d'
A
A
R
58a
R
C
FET 11
FET 12
FET 13
FET 14
FET 21
FET 22
FET 23
FET 24
ld11
ld12
ld12
ld11
ld21
ld22
ld22
ld21
58a
58b
58c
58d
l21
52a
l22
52b
l23/2
52c'
l23/2
52c"
l21
52e
l22
52d
l23/2
52c"
l21
52e
52'
52
52"
54a
54b
54c
54d
36
36
57
VD
57a
57b

FIG. 3

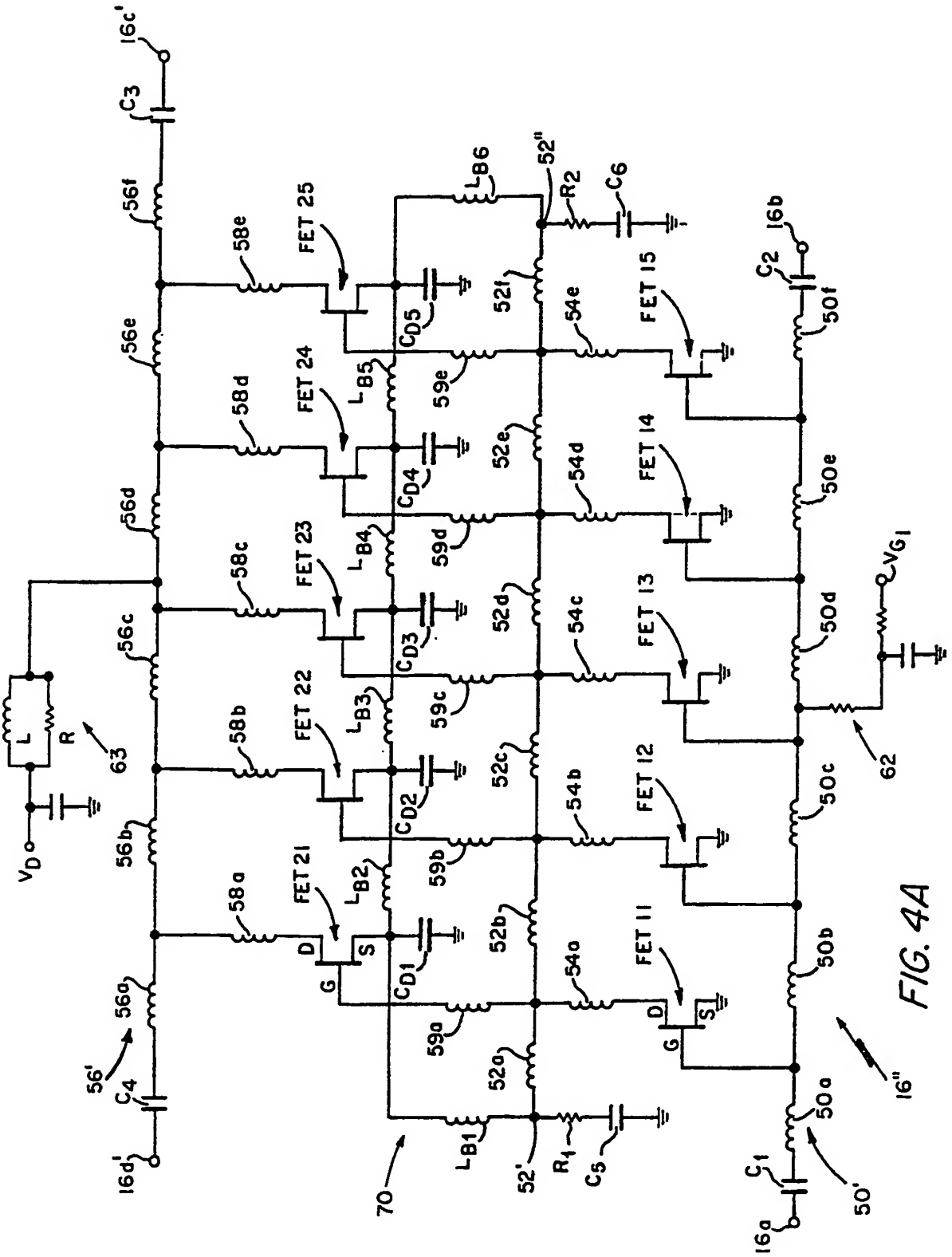
16c'
C3
56f
58e
FET 25
LB6
52"
R2
C6
16b
C2
50f
FET 15
54e
52f
CD5
59e
LB5
FET 24
58d
56e
52e
54d
FET 14
50e
CD4
59d
LB4
FET 23
58c
56d
52d
54c
FET 13
50d
VG1
CD3
59c
LB3
FET 22
58b
56c
52c
54b
FET 12
50c
62
CD2
59b
LB2
FET 21
58a
56b
52b
54a
FET 11
50b
CD1
59a
52a
56a
56'
C4
16d'
70
LB1
52'
R1
C5
C1
16a
50'
16"
63
L
R
VD

FIG. 4A

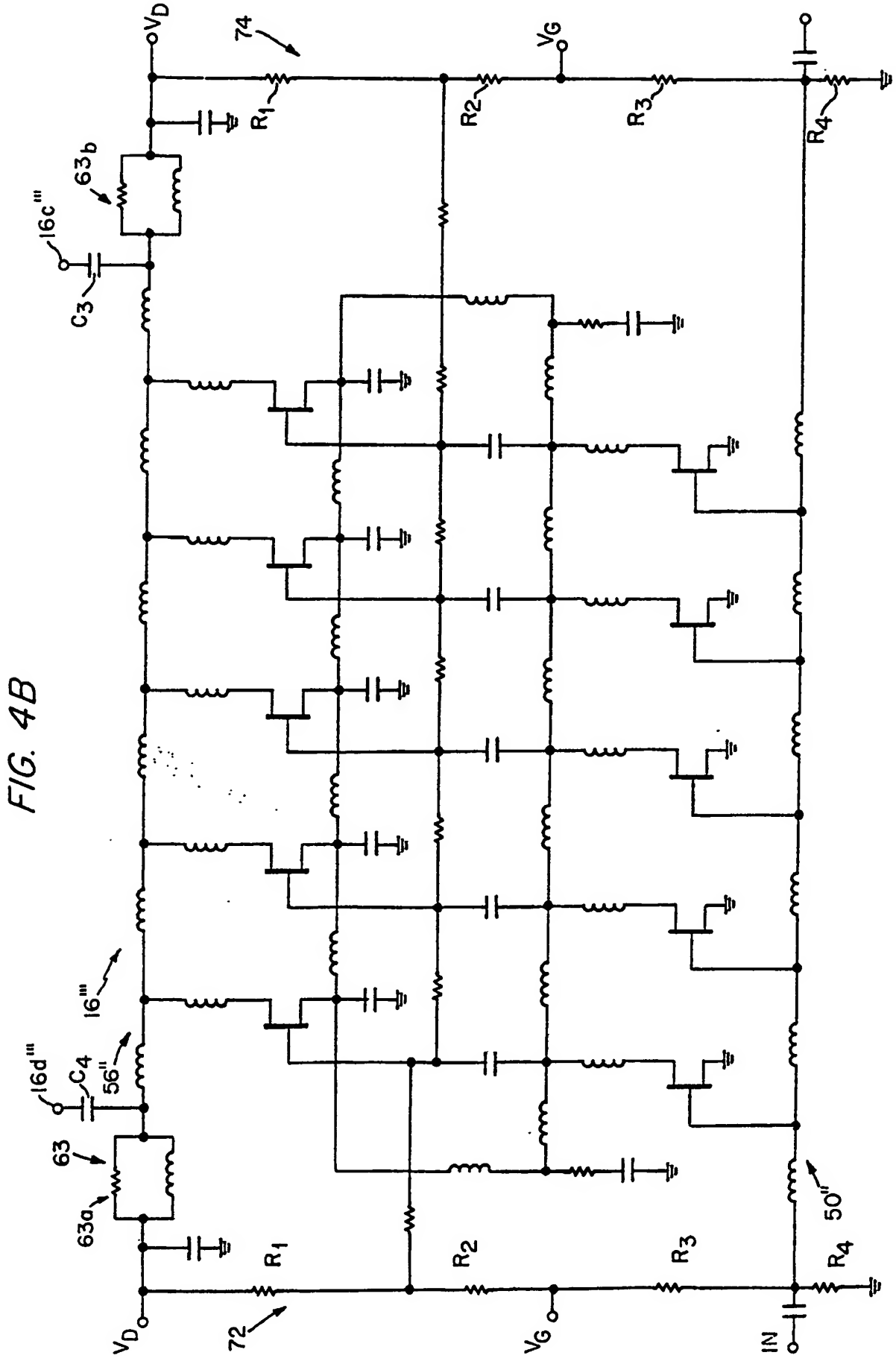

FIG. 4B

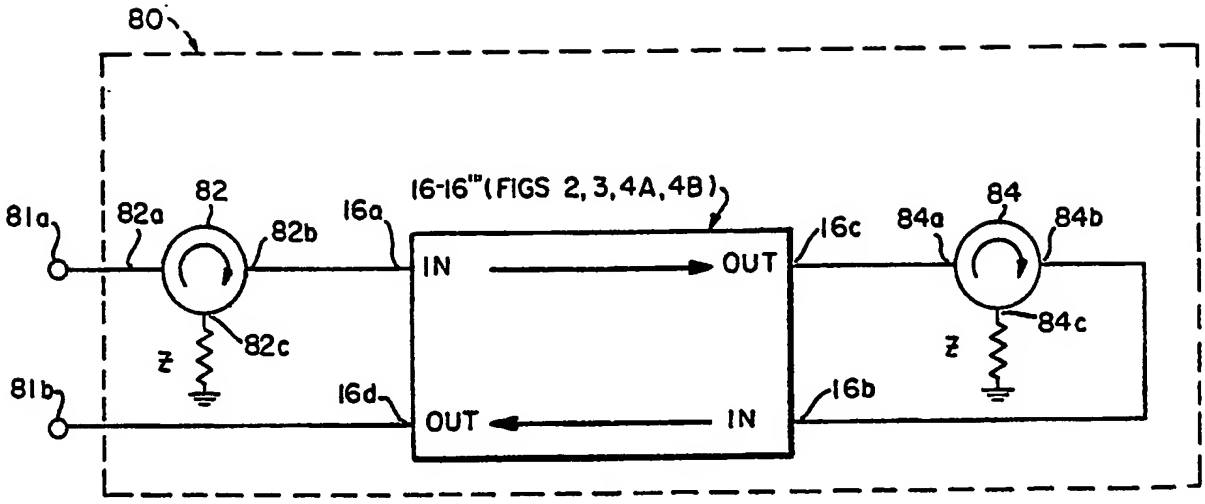

FIG. 5

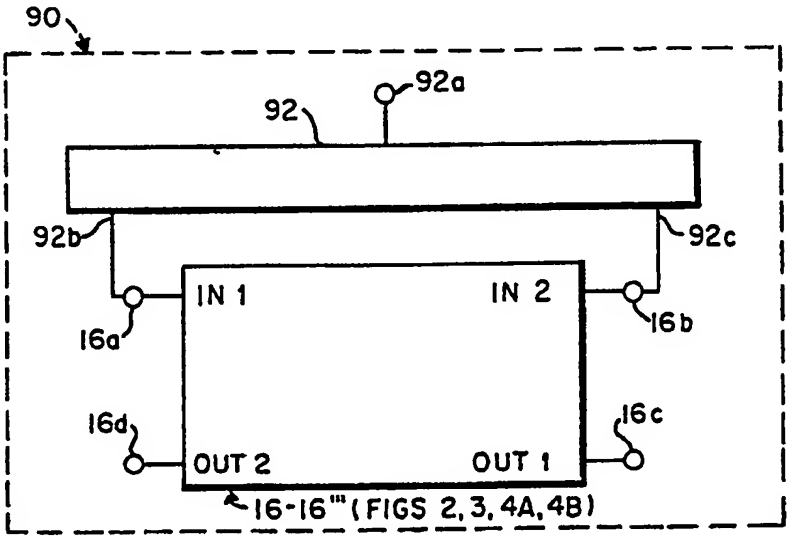

FIG. 6

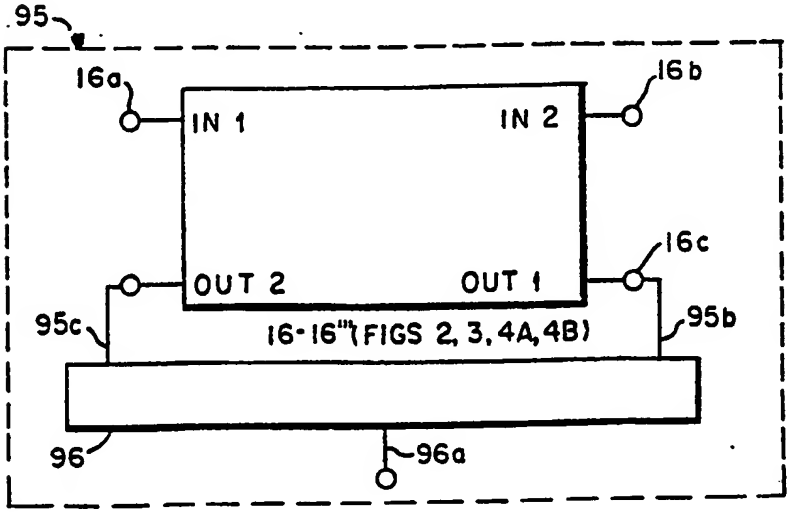

FIG. 7

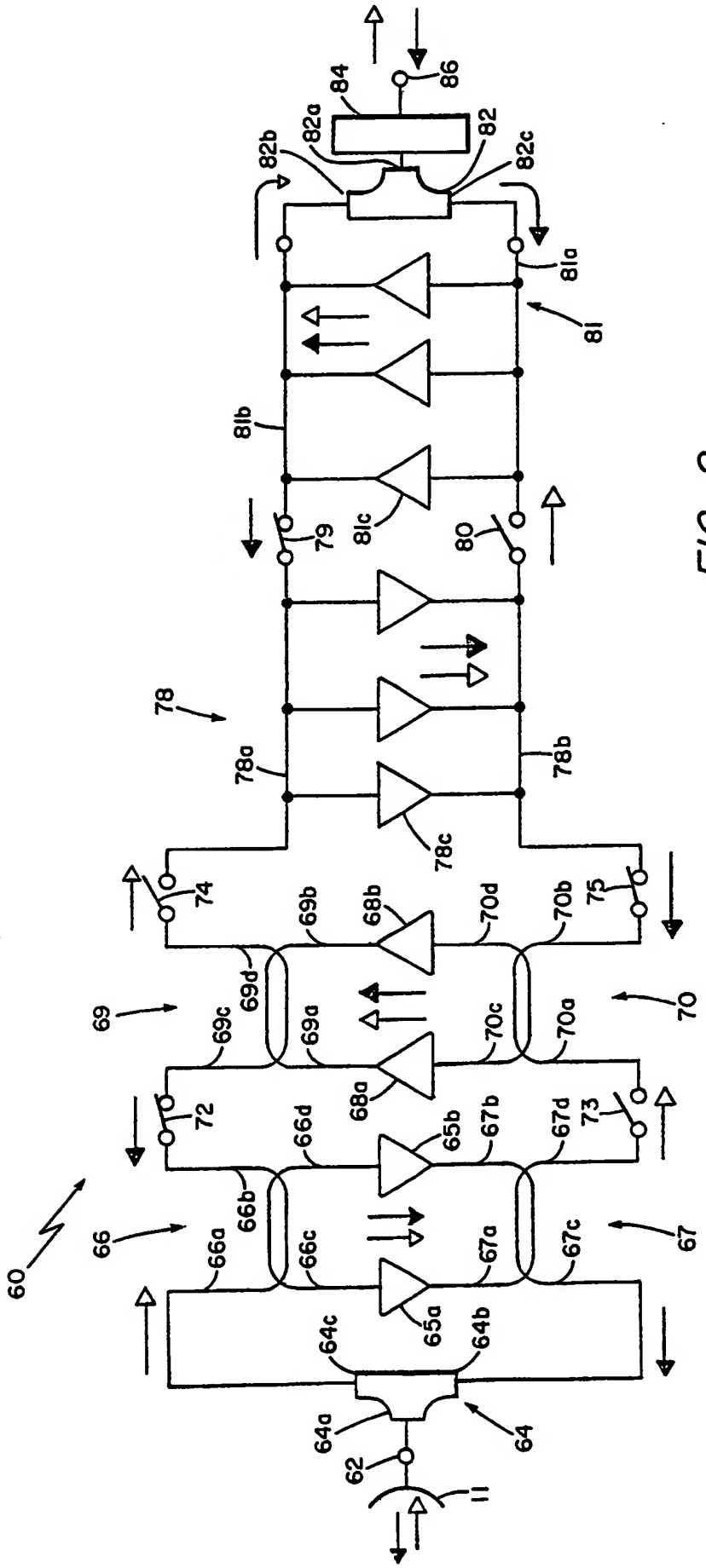
84
86
82a
82
82b
82c
81a
81
81b
81c
79
80
78
78a
78b
78c
74
75
69b
68b
70d
70b
69d
69
69c
69a
70c
70a
70
72
68a
73
66d
65b
67b
67d
66b
66
66a
66c
67a
67c
67
60
65a
64c
64b
64a
64
62
11

FIG. 8